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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bryan R. White
Serial No. : 09/676,844
Filed : September 29, 2000
Title : SHARED TRANSLATION ADDRESS CACHING

Art Unit : 2676
Examiner : Mackly Moonestime

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REPLY TO ACTION OF JUNE 11, 2003

(Assignee: Intel Corporation)

In reply to the Final Office Action of June 11, 2003, Applicant submits the following remarks.

Claims 1-16 are pending. Claims 1, 7, and 13 are the independent claims.

Independent claims 1, 7, and 13 stand rejected as allegedly obvious over U.S. Patent No. 6,480,200 ("Fisher") in view of U.S. Patent No. 6,374,317 ("Ajonovic").

Claim 1 recites:

> A memory controller hub comprising:
> an internal graphics subsystem adapted to perform graphics operations on data; and
> a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and available to an external graphics controller coupled to the memory controller hub to store graphics data.

Thus, the same cache is used for storing physical memory addresses available for use by an internal graphics subsystem and for storing physical memory addresses available for use by an external graphics controller. As explained in the applicant's specification, the cache may be used to store Graphics Address Remapping Table (GART) entries (used by the external graphics controller in AGP mode) or Graphics Translation Table (GTT) entries (used by the internal graphics subsystem in Gfx mode). GART and GTT entries are used for translating virtual memory addresses into physical memory addresses. The specification explains an advantage of having a single cache that can store both GART and GTT entries: "Since the number of GART entries or GTT entries that may be stored in TLB 28 is limited by the physical die area size of the TLB, using the same TLB to store GART entries in AGP mode and to store GTT entries in Gfx mode effectively doubles the number of GART or GTT entries that may be stored in TLB